



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

| APPLICATION NO.   | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO.  | CONFIRMATION NO. |
|---|-------------|----------------------|----------------------|------------------|
| 09/823,299  | 03/30/2001  | Rahul Magoon         | 50321-1920           | 6843             |
| 24504   | 7590        | 05/05/2005           | EXAMINER             |                  |
| THOMAS, KAYDEN, HORSTEMEYER & RISLEY, LLP<br>100 GALLERIA PARKWAY, NW<br>STE 1750<br>ATLANTA, GA 30339-5948 |             |                      | WILLIAMS, LAWRENCE B |                  |
|   |             |                      | ART UNIT             | PAPER NUMBER     |
|   |             |                      | 2634                 |                  |

DATE MAILED: 05/05/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

## Office Action Summary

Application No.

09/823,299

Applicant(s)

MAGOON ET AL.

Examiner

Lawrence B Williams

Art Unit

2634

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 03 November 2004.  
2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.  
3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1-28 is/are pending in the application.  
4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.  
5) ☒ Claim(s) 25-28 is/are allowed.  
6) ☒ Claim(s) 1-10 and 13-22 is/are rejected.  
7) ☒ Claim(s) 11, 12, 23 and 24 is/are objected to.  
8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.  
10) ☒ The drawing(s) filed on 01 November 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).  
11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
a) ☐ All b) ☐ Some \* c) ☐ None of:  
1. ☐ Certified copies of the priority documents have been received.  
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).  
\* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892)  
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)  
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_.  
4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date \_\_\_\_\_.  
5) ☐ Notice of Informal Patent Application (PTO-152)  
6) ☐ Other: \_\_\_\_\_.

## **DETAILED ACTION**

### ***Response to Arguments***

1. Applicant's arguments filed 14 February 2005 have been fully considered but they are not persuasive. Examiner maintains previous rejections. Applicant asserts (Discussion of the Rejection, pg. 15, lines 10-15) that Havens et al. (US Patent 6,313,680) does not disclose the emphasized features of a filter that produces an output, and a variable resistance across the output. Examiner respectfully disagrees. Havens et al. discloses in Fig. 4, the emphasized features of the claim. Havens et al. Fig. 4 discloses a "a first phase splitting filter (302) that produces a first output (106); and a first variable resistance (R1) connected across the first output (col. 3, lines 12-24). Therefore the rejections of claims 1-10 and 13-22 are maintained.

### ***Claim Rejections - 35 USC § 102***

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-7, 9, 10, 13-22 are rejected under 35 U.S.C. 102(b) as being anticipated by Havens et al. (US Patent 6,313,680 B1).

(1) With regard to claim 1, Havens et al. discloses in Fig(s). 3, 4, a polyphase filter comprising a first phase splitting filter (302) that produces a first output (106), a second phase splitting filter (302) that produces a second output (108), a first variable resistance (R1)

connected across the first output (Fig. 4; col. 3, lines 17-20), and circuitry (402) capable of detecting the phase of the outputs produced by the first and second outputs, and circuitry capable of adjusting the first variable resistance to produce a desired phase difference between the first output and the second output (col. 6, lines 1-27).

(2) With regard to claim 2, Havens et al. also discloses wherein the first output and the second output are single-ended outputs (col. 5, lines 29-31).

(3) With regard to claim 3, Havens et al. also discloses in Fig. 6, wherein the first and the second outputs are differential outputs (col. 5, lines 31-35).

(4) With regard to claim 4, Havens et al. also discloses in Fig. 4, the filter comprising a second variable resistance (R2) connected across the second output.

(5) With regard to claim 5, Havens et al. also discloses in Fig. 5, wherein the first variable resistance (Q1) and the second variable resistances (Q2) include transistors.

(6) With regard to claim 6, Havens et al. also discloses wherein the transistors including at least one MOSFET transistor operating in the linear range (col. 5, lines 24-26).

(7) With regard to claim 7, Havens et al. also discloses wherein the first variable resistance and the second variable resistance include a bipolar differential pair (col. 6, lines 42-51).

(8) With regard to claim 9, claim 9 inherits all limitations of claim 1 above. Furthermore, Havens et al. also discloses in Figs. 3 and 8 wherein the circuitry capable of detecting the phase of the outputs includes a phase detector, an integrator and a differential amplifier (col. 6, lines 1-13; col. 7, lines 28-37).

(9) With regard to claim 10, Havens et al. also discloses wherein the circuitry capable of detecting the phase of the outputs includes a phase detector, an integrator, a differential amplifier, a capacitor and a controller for selectively storing and holding the output of the differential amplifier in the capacitor (col. 5, line 36- col. 6, line 27).

(10) With regard to claim 13, Havens et al. discloses in Fig(s). 3, 4, a polyphase filter comprising a first phase splitting filter (302) that produces a first output (106), a second phase splitting filter (302) that produces a second output (108), a first variable resistance (R1) connected across the first output, and a detector (402) that determines the phase of the first and second outputs, and adjusts the first variable resistance to produce a desired phase difference between the first output and the second output (col. 6, lines 1-27).

(11) With regard to claim 14, claim 14 inherits all limitations of claim 13 above. Furthermore, Havens et al. also discloses wherein the first output and the second output are single-ended outputs (col. 5, lines 29-31).

(12) With regard to claim 15, claim 15 inherits all limitations of claim 13 above. Furthermore, Havens et al. also discloses in Fig. 6, wherein the first and the second outputs are differential outputs (col. 5, lines 31-35).

(13) With regard to claim 16, claim 16 inherits all limitations of claim 13 above. Furthermore, Havens et al. also discloses in Fig. 4, the filter comprising a second variable resistance (R2) connected across the second output.

(14) With regard to claim 17, claim 17 inherits all limitations of claim 16 above. Furthermore, Havens et al. also discloses in Fig. 5, wherein the first variable resistance (Q1) and the second variable resistances (Q2) include transistors.

(15) With regard to claim 18, claim 18 inherits all limitations of claim 17 above. Furthermore, Havens et al. also discloses wherein the transistors including at least one MOSFET transistor operating in the linear range (col. 5, lines 24-26).

(16) With regard to claim 19, claim 19 inherits all limitations of claim 16 above. Furthermore, Havens et al. also discloses wherein the first variable resistance and the second variable resistance include a bipolar differential pair (col. 6, lines 42-51).

(17) With regard to claim 20, though Havens et al. does not teach wherein the first variable resistance and the second variable resistance include a digitally switchable resistance pair, this limitation would be merely a design choice to one skilled in the art to incorporate the many advantages of digital technology.

(18) With regard to claim 21, claim 21 inherits all limitations of claim 13 above. Furthermore, Havens et al. also discloses in Figs. 3 and 8 wherein the detector includes a phase detector, an integrator and a differential amplifier (col. 6, lines 1-13; col. 7, lines 28-37).

(19) With regard to claim 22, claim 22 inherits all limitations of claim 13 above. Furthermore, Havens et al. also discloses wherein the detector includes a phase detector, an integrator, a differential amplifier, a capacitor and a controller for selectively storing and holding the output of the differential amplifier in the capacitor (col. 5, line 36- col. 6, line 27).

### ***Claim Rejections - 35 USC § 103***

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person

Art Unit: 2634

having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claim 8 is rejected under 35 U.S.C. 102(b) as anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over Havens et al. (US Patent 6,313,680 B1).

Though Havens et al. does not teach wherein the first variable resistance and the second variable resistance include a digitally switchable resistance pair, this limitation would be merely a design choice to one skilled in the art to incorporate the many advantages of digital technology.

*Allowable Subject Matter*

6. Claims 25-28 are allowed.

7. Claims 11, 12, 23, 24 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

8. The following is a statement of reasons for the indication of allowable subject matter: the instant application discloses communication system and method for obtaining accurate quadrature separation of phase components. A search of prior art records fail to disclose a method or system “wherein a local oscillator provides a fixed frequency signal to inputs of the first phase splitting filter and the second phase splitting filter, an RF test signal source provides a test signal which is mixed with the first output and the second output to produce an I-based band signal and a Q-based band signal” as disclosed in claims 11-12, 23-24. The prior art also does not teach a communication system wherein “the receiver comprising an RF input, a local oscillator, a polyphase filter connected to an output of the local oscillator, the polyphase filter

producing first and second outputs from the local oscillator output, a mixer that combines the RF input with the first and second outputs of the polyphase filter, baseband circuitry, an analog-to-digital converter, and a digital signal processor that demodulates an output of the analog-to-digital converter, and produces a demodulated output” or “splitting the local oscillator frequency into two signals having a predetermined phase difference to produce a first output and a second output, mixing the first output and the second output with a radio frequency test signal to generate an I baseband signal and a Q baseband signal; detecting the phase difference between the I baseband signal and the Q baseband signal; and adjusting the phase difference of the first output and/or the second output to produce a desired phase difference between the I baseband signal and the Q baseband signal as disclosed in claims 25 and 28, respectively.

### ***Conclusion***

9. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.



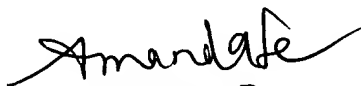
10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lawrence B Williams whose telephone number is 571-272-3037. The examiner can normally be reached on Monday-Friday (8:00-5:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Stephen Chin can be reached on 571-272-3056. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Lawrence B. Williams

lbw  
April 26, 2005

  
**AMANDA T. LE**  
**PRIMARY EXAMINER**